UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte HARI K. RAVICHANDRAN

Appeal No. 2006-2441
Application No. 10/056,224

ON BRIEF

Before HAIRSTON, MACDONALD, and HOMERE, ***Administrative Patent Judges***.

HOMERE, ***Administrative Patent Judge***.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the final rejection of claims 9 through 19, all of which are pending in this application.

We reverse.

Invention

Appellant's invention relates generally to a method for monitoring the execution of a program. Upon receipt of a first address indicator, a probe logic circuit (108) searches a first memory device (106) associated with the address indicator. If the search produces no entry, the probe logic circuit (108) generates a probe signal to indicate a miss entry in the first memory device. Further, a temporal identifier signal is generated for association with the probe signal for each address entry not found in the first memory device. Finally, the temporal identifier signals and the corresponding probe signals are then stored in memory.

Claim 9 is representative of the claimed invention and is reproduced as follows:

> 9. A method for monitoring an execution of a program, the method comprising the steps of:
>
> (1) obtaining a first indication including a first address;
>
> (2) searching a first memory device for an entry associated with the first address;
>
> (3) when the entry in the first memory device does not exist, generating at least one probe signal indicating a miss entry in the first memory device;

(4) generating a temporal identifier signal that is associated with the probe signals; and

(5) storing the temporal identifier signal and the probe signals in memory.

References

The Examiner relies on the following references:

Razban	5,289,587	Feb. 22, 1994
Bunnell	5,564,015	Oct. 8, 1996
Roeber et al. (Roeber)	5,682,328	Oct. 28, 1997 (filed on Sep. 11, 1996)
Mahalingaiah et al. (Mahalingaiah)	5,933,626	Aug. 3, 1999 (filed on June 12, 1997)
Levine et al. (Levine)	6,067,644	May 23, 2000 (filed on Apr. 15, 1998)

Rejections At Issue

A. Claim 9 stands rejected under 35 U.S.C. § 103 as being unpatentable over the combination of Bunnell and Roeber.

B. Claim 10 stands rejected under 35 U.S.C. § 103 as being unpatentable over the combination of Bunnell, Roeber and Razban.

C. Claim 11 stands rejected under 35 U.S.C. § 103 as being unpatentable over the combination of Bunnell, Roeber and Levine.

D. Claim 12 stands rejected under 35 U.S.C. § 103 as being unpatentable over the combination of Bunnell, Roeber and Mahalingaiah.

E. Claims 13 and 14 stand rejected under 35 U.S.C. § 103 as being unpatentable over the combination of Bunnell, Roeber and Levine.

F. Claims 15 through 17 stand rejected under 35 U.S.C. § 103 as being unpatentable over the combination of Bunnell, Roeber, Levine, Razban and Mahalingaiah.

G. Claims 18 and 19 stand rejected under 35 U.S.C. § 103 as being unpatentable over the combination of Bunnell, Roeber, Levine and Razban.

Rather than reiterate the arguments of Appellant and the Examiner, the opinion refers to respective details in the Briefs[1] and the Examiner's Answer[2]. Only those arguments actually made by Appellant have been considered in this decision. Arguments that

[1] Appellant filed an Appeal Brief on October 28, 2005. Appellant filed a Reply Brief on May 15, 2006.
[2] The Examiner mailed an Examiner's Answer on March 27, 2006. The Examiner mailed an office communication on June 02, 2006 stating that the Reply Brief has been entered and considered. ~~December 16, 2004 has not been considered.~~

Appellant could have made but chose not to make in the Briefs have not been taken into consideration. See 37 CFR 41.37(c)(1)(vii)(eff. Sept. 13, 2004).

OPINION

In reaching our decision in this appeal, we have carefully considered the subject matter on appeal, the Examiner's rejections, the arguments in support of the rejections and the evidence of obviousness relied upon by the Examiner as support for the rejections. We have, likewise, reviewed and taken into consideration Appellant's arguments set forth in the Briefs along with the Examiner's rationale in support of the rejections and arguments in the rebuttal set forth in the Examiner's Answer.

After full consideration of the record before us, we do not agree with the Examiner that claim 9 is properly rejected under 35 U.S.C. § 103 as being unpatentable over the combination of Bunnell and Roeber. We also do not agree with the Examiner that claims 10 through 19 are properly rejected over the various combinations of Bunnell and Roeber, Levine, Razban and/or Mahalingaiah. Accordingly, we reverse the Examiner's rejections of claims 9 through 19 for the reasons set forth **infra**.

Under 35 U.S.C. § 103, is the Rejection of Claim 9 as being unpatentable over the combination of Bunnell and Roeber Proper?

In rejecting claims under 35 U.S.C. § 103, the Examiner bears the initial burden of establishing a **prima facie** case of obviousness. **In re Oetiker**, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). **See also In re Piasecki**, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984). The Examiner can satisfy this burden by showing that some objective teaching in the prior art or knowledge generally available to one of ordinary skill in the art suggests the claimed subject matter. **In re Fine**, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). Only if this initial burden is met does the burden of coming forward with evidence or argument shift to the Appellants. **Oetiker**, 977 F.2d at 1445, 24 USPQ2d at 1444. **See also Piasecki**, 745 F.2d at 1472, 223 USPQ at 788. Thus, the examiner must not only assure that the requisite findings are made, based on evidence of record, but must also explain the reasoning by which the findings are deemed to support the examiner's conclusion. However, a suggestion, teaching, or motivation to combine the relevant prior art teachings does not have to be found explicitly in the prior art, as the teaching, motivation, or suggestion may be implicit from the prior art as a whole, rather than expressly

stated in the references. The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art. ***In re Kahn***, 441 F.3d 977, 987-88, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006) citing **In re Kotzab**, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1316-17 (Fed. Cir. 2000). See also **In re Thrift**, 298 F.3d 1357, 1363, 63 USPQ2d 2002, 2008 (Fed. Cir. 2002).

An obviousness analysis commences with a review and consideration of all the pertinent evidence and arguments. "In reviewing the [E]xaminer's decision on appeal, the Board must necessarily weigh all of the evidence and argument." **Oetiker**, 977 F.2d at 1445, 24 USPQ2d at 1444. "[T]he Board must not only assure that the requisite findings are made, based on evidence of record, but must also explain the reasoning by which the findings are deemed to support the agency's conclusion." **In re Lee**, 277 F.3d 1338, 1344, 61 USPQ2d 1430, 1434 (Fed. Cir. 2002).

With respect to representative claim 1, Appellant argues in the Appeal Brief and the Reply Brief that the combination of Bunnell and Roeber does not teach generating a temporal identifier for association with a probe signal, and subsequently

storing the probe signals with associated temporal identifiers. Particularly, at pages 4 and 5 of the Appeal Brief, Appellant states the following:

> However, Bunnell and Roeber, taken alone or in combination, do not teach or suggest a method for monitoring an execution of a program which includes when the entry in the first memory device does not exist, generating at least one probe signal indicating a miss entry in the first memory device; generating a temporal identifier signal that is **associated with the probe signals; and storing the temporal identifier signal and the probe signals** in memory.

In order for us to decide the question of obviousness, "[t]he first inquiry must be into exactly what the claims define." **In re Wilder**, 429 F.2d 447, 450, 166 USPQ 545, 548 (CCPA 1970). "Analysis begins with a key legal question-- what is the invention claimed ?"...Claim interpretation...will normally control the remainder of the decisional process." **Panduit Corp. v. Dennison Mfg.**, 810 F.2d 1561, 1567-68, 1 USPQ2d 1593, 1597 (Fed. Cir. 1987).

We note that representative claim 9 reads in part as follows:

> [G]enerating a temporal identifier signal that is associated with the probe signals; and storing the temporal identifier signal and the probe signals in memory.

We note that at pages 4 and 5, paragraphs 17 and 18, Appellant's specification states the following:

> 0017] The performance monitor circuit 112 provides the capability of collecting probe data signals and associating a temporal identifier, such as a time stamp, to the probe data signals. (Emphasis added).
>
> [0018] FIG. 2 illustrates the probe signals in an embodiment of the present invention. The performance monitor circuit 112 can receive three signals: (1) a first signal 134 indicating the value of a program counter (PC); (2) a second signal 136 indicating a device identifier; and (3) a third signal 138 representing the number of misses that the identified device has incurred thus far. The performance monitor circuit 112 associates a time stamp signal 132 with these signals and stores their values in the second memory 110. Preferably, the second memory 110 is used to store data from the performance monitor circuit 112 only. The time stamp signal 132 can be 16 bits wide, the program counter signal 134 can be 32 bits wide, the miss identifier signal 136 can be 4 bits wide, and the miss counter signal 138 can be 16 bits wide as shown in FIG. 2. The signals show in FIG. 2 are herein referred to as the probe data or probe data signals.

Thus, the claim does require generating a temporal identifier for association with a probe signal, and subsequently storing the probe signals with associated temporal identifiers.

Now, the question before us is what Bunnell and Roeber would have taught to one of ordinary skill in the art? To answer this question, we find the following facts:

1. At column 6, line 44 through column 7, line 5, Bunnell states:

> The microprocessor 20 communicates to the CPU activity monitor 24 via a cache miss signal 36 and a plurality of mode signals 38, 40, and 42, an address bus 32, and a data bus 34. As explained in more detail below, the plurality of mode signals include a read/write signal 38, a data/control

signal 40, and a memory/IO signal 42 that communicate the operating mode of the microprocessor 20.

The cache memory system 30 generates the cache miss signal 36 when the microprocessor 20 must access the main memory 22. Whenever the CPU 28 requests data, the cache memory system 30 checks to see if data already exists in the cache memory system 30 (a hit). If the data does not exist in the cache memory system 30 (a miss), the CPU 28 accesses the main memory 22. Thus, the cache memory system 30 generates the cache miss signal 36 when the CPU 28 accesses data that is not stored in the cache memory system 30.

The CPU activity monitor 24 monitors the number of CPU activity events that occur during a certain time interval. In the preferred embodiment, the duration of the time interval has a range of one to tens of milliseconds. The clock 26 which generates a clock signal 44 is a system clock or a division of the system clock. The CPU activity monitor 24 uses the cache miss signal 36, the clock signal 44, and the plurality of mode signals 38, 40, and 42 to generate an interrupt request 46. The interrupt request 46 connects to the microprocessor 20 and initiates a power system interrupt service routine.

2. At column 3, lines 24 through 42, Roeber states:

According to the invention, an event logging mechanism is effected as a hybrid implementation having hardware and software components. The event logging mechanism's hardware component includes an off-the-shelf single board computer or control card configurable onto a backplane containing the target processor(s) being monitored. A high resolution clock on the control card is used to time stamp events. A portion of memory on the control card is used as a central buffer to store event data, while another portion of memory on the control card is used to store a control program that effects functionality of the control card. The central buffer of memory resident on the control card is used to collect event records from the target processor(s) for transfer to one or more host systems for post processing of event data. The

> control card includes a network interface to facilitate communication between the host computer(s) used for post processing of event data and to control, communicate with and access the control card.

With the above discussion in mind, we find that the combination of Bunnell and Roeber does not teach the claimed invention. We find that Bunnell teaches a device for monitoring CPU accesses to the main memory (22). Particularly, Bunnell teaches a CPU (28) and a cache memory (30) connected to a CPU activity monitor (24) via a cache miss signal (36). Whenever the CPU requests data, the cache memory checks its internal memory for the requested data. If the data is not available in the cache, it issues a miss signal, and the CPU accesses the main memory for the requested data. Bunnell also teaches that the CPU activity monitor receives a clock signal, a cache miss signal and a plurality of modes signals to determine when the CPU transitions from an active to an inactive state and vice-versa. Next, we find that Roeber teaches an event logging mechanism having a central memory for storing user-designated events data and time-stamps associated therewith. It is our view that one of ordinary skill in the art would have duly realized that Roeber's teachings do not complement Bunnell's teachings to yield the invention as set forth in representative claim 9. Particularly,

the ordinarily skilled artisan would have readily been apprised of the fact that Bunnell's teaching of the CPU monitoring device is limited to monitoring CPU data access to main memory when a requested data is not available in the cache memory. Bunnell indicates that the CPU monitoring device uses the cache signals, inter alia, to determine when the computer is in transition from an active to inactive state vice-versa. See column 4, lines 44 through 49. The ordinarily skilled artisan would have also recognized that even though Bunnell teaches the issuance of a miss entry when the requested data is not available in the cache, it does not particularly teach keeping a log of such missed entries, let alone generating and storing temporal identifiers (time stamps) indicating the time of such missed entries. Further, in stark contrast with the Examiner's interpretation, we note that the ordinarily skilled artisan would have recognized that Bunnell's teaching of a system clock does not lend itself to generating and storing such temporal identifiers. Additionally, it is our view that albeit Roeber teaches a central log for recording events and time stamps associated therewith, such recording is not taught in conjunction with cache misses. Thus, at the time of the invention, the ordinarily skilled artisan

would not have looked to the teachings of Roeber in order to cure the deficiencies of Bunnell. Consequently, we find error in the Examiner's stated position, which concludes that the combination of Bunnell and Roeber teaches the step of generating a temporal identifier for association with a probe signal, and subsequently storing the probe signals with associated temporal identifiers. It is therefore our view, after consideration of the record before us, that the evidence relied upon and the level of skill in the particular art would have not suggested to the ordinarily skilled artisan the invention as set forth in claim 9. Accordingly, we will not sustain the Examiner's rejection of claim 9.

With regard to claims 10 through 19, Appellant argues at pages 5 and 6 of the Appeal Brief that the combination of Bunnell and Roeber does not teach or suggest the claimed limitation of generating a temporal identifier for association with a probe signal, and subsequently storing the probe signals with associated temporal identifiers. We have already addressed this argument in the discussion of claim 9 above, and we agree with Appellant. Further, Appellant argues that neither Levine nor Razban, nor Mahalingaiah cures the noted deficiencies of the

Bunnell-Roeber combination. Our review of the cited references indicates they are not concerned with providing a temporal identifier for each miss entry in a cache. One of ordinary skill in the art, at the time of the present invention, would have thus not found that these teachings, taken alone or in combination, complement the Bunnell-Roeber's system to yield the claimed step of generating a temporal identifier for association with a probe signal, and subsequently storing the probe signals with associated temporal identifiers. It is therefore our view, after consideration of the record before us, that the evidence relied upon and the level of skill in the particular art would not have suggested to the ordinarily skilled artisan the invention as set forth in claims 10 through 19. Accordingly, we will not sustain the Examiner's rejection of claims 10 through 19.

CONCLUSION

In view of the foregoing discussion, we have not sustained the Examiner's decision rejecting claims 1 through 19 under 35 U.S.C. § 103. Therefore, we reverse.

REVERSED

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